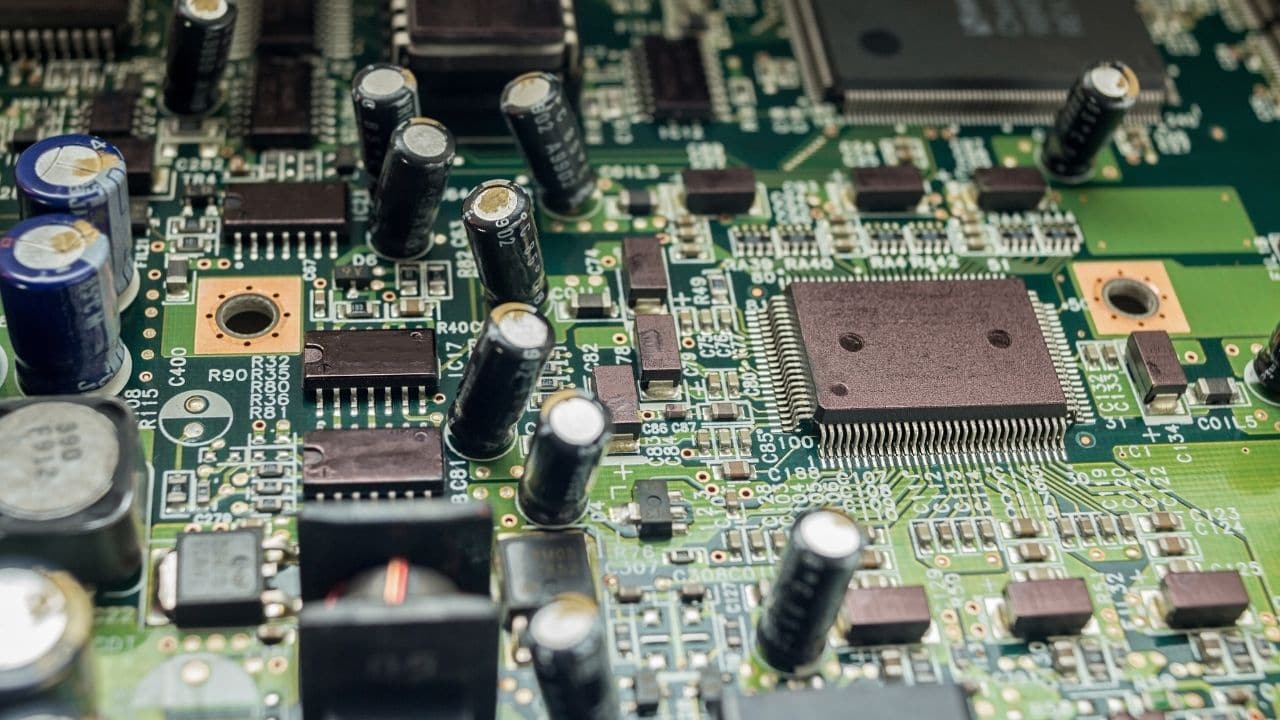
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| **Personal Inforamtion**  **Name : Muhammad Huzaifa Khan**  **F.Name : Muhammad Nawab Khan**  **Roll # : 49**  **Class : BSSE- 1st Semester** |
| **Course Information**  **Teacher : Miss Madiha Khurram**  **Course : Computer Logic Design**  **Course# : CSSE-303** |

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**PRACTICAL # 01**

**OBJECTIVE:**

To study the operations of Basic Gate i.e. AND, OR, NOT

**ICS:**

For AND: IC 74LS08

For OR: IC 74LS32

For NOT: IC 74LS04

**Apparatus:**

* Bread board
* LED
* wires
* DC supply

**PROCEDURE:**

FOR AND / OR: First Connect ICS 74LS08 / 74LS32 to the Breadboard and then connect wires from pin 7 and pin 14 to the ground and power respectively. Now for input, connect wires to pin 1 and pin 2 and place a LED with pin 3. Remember, shorter end connect with negative and longer end connect with positive. Now provide input to the wires connected to pin # 1 and 2 as per the following truth table

FOR NOT: Firstly connect IC74LS04 to the breadboard and then connect wires from pin 7 and pin 14 to the ground and power respectively. Now for inputs, connect wire to pin 1 and place a LED with pin 2. Remember, shorter end connects with negative and longer end connect with positive. Now provide input to the wire connected to pin # 1 as per the following truth table

**Truth Table:**

AND GATE

|  |  |  |
| --- | --- | --- |
| INPUT: A | INPUT: B | OUTPUT: A.B |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

OR GATE

|  |  |  |
| --- | --- | --- |
| INPUT: A | INPUT: B | OUTPUT: A+B |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

NOT GATE

|  |  |
| --- | --- |
| INPUT: A | OUTPUT: |
| 0 | 1 |
| 1 | 0 |

**GATE Symbols:**

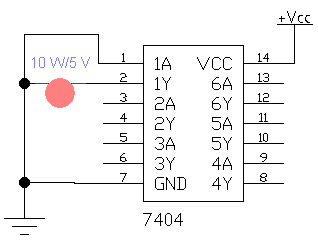
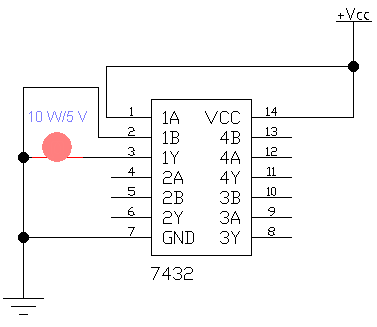
AND GATE

****

NOT GATE

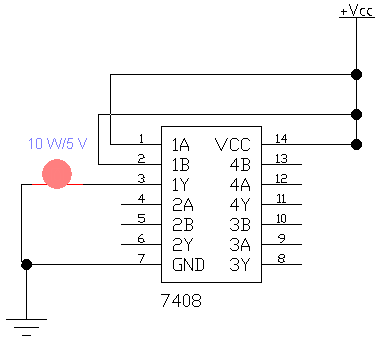
OR GATE

****

**Circuit Diagram:**

OR GATE

NOT GATE

****

AND GATE

**Result:**

AND GATE: The LED turns on when we give 1, 1 to a and b otherwise off

OR GATE: The LED turns off only when we give 0,0 to a and b otherwise off

NOT GATE: LED turns on when we give 1 to a

**PRACTICAL # 2**

**OBJECTIVE:**

To study the combination of Basic Gate i.e. AND, OR using following equation:

* **A.B + B.C + B.D**
* **A.B + (C + D).B**

**ICS:**

* IC 74LS08 (AND GATE)
* IC 74LS32 (OR GATE)

**Apparatus:**

* Bread board
* LED
* wires
* DC supply

**Procedure:**

FOR A.B + B.C + B.D

Firstly place two ICS, that is 74LS08 and 74LS32, on bread board and then connect pin 7 and pin 14 of each IC to ground and power respectively. In 74LS08, connect wires to pin 1, pin 2, pin 5 and pin 9 for inputs A, B, C and D respectively and also take input B from pin 2 to pin 4 and pin 10 and then we have A.B on pin 3, B.C on pin 6 and B.D on pin 8. Now, from IC 74LS08, take A.B, B.C, B.D as input to pin 1, pin 2 and pin 5 of IC 74LS32 respectively. Now, in IC74LS32, we have (A.B) + (B.C) on pin 3 which we give to pin 4 as input. In last we have (A.B) + (B.C) + (B.D) on pin 6 where we connect LED. Remember, shorter end connects with negative and longer end connect with positive. Now, As per following truth table, provide input to the wire connected to pin # 1, 2, 5 and 9 of IC 74LS08 as A, B, C and D respectively.

FOR A.B + (C + D).B:

Firstly place two ICs that is 74LS08 and 74LS32, on bread board. Connect inputs A to 1st pin of AND gate, B to 2nd and 9th pin of AND gate, C to 1st pin of OR gate and D to 2nd pin of OR gate. Connect 3rd pin, which contain C+D to 10th pin of AND gate. Connect 8th pin of AND gate, which contain (C+D).B, to 4th pin of OR gate. Connect 3rd pin of AND gate, which contain A.B, to 5th pin of OR gate. At last, connect bulb to 6th pin of OR gate. Now provide inputs A,B, C and D according to the following truth tables.

**Truth Table:**

FOR A.B + B.C + B.D:

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **A.B** | **B.C** | **B.D** | **A.B + B.C + B.D** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

FOR A.B + (C + D).B

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **A.B** | **C+D** | **(C+D).B** | **A.B + (C+D).B** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**GATE Symbols:**

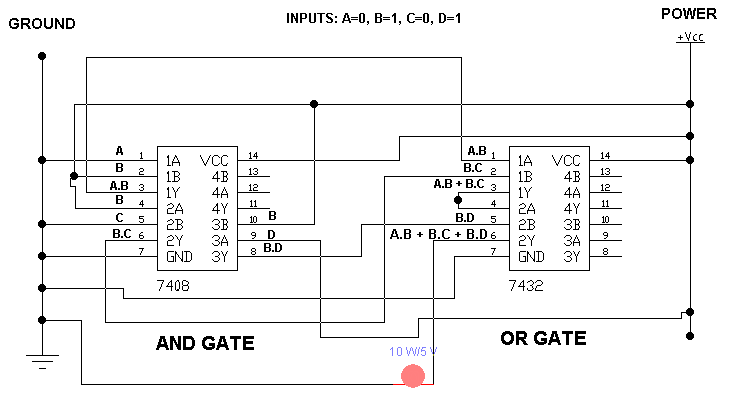
****

OR GATE

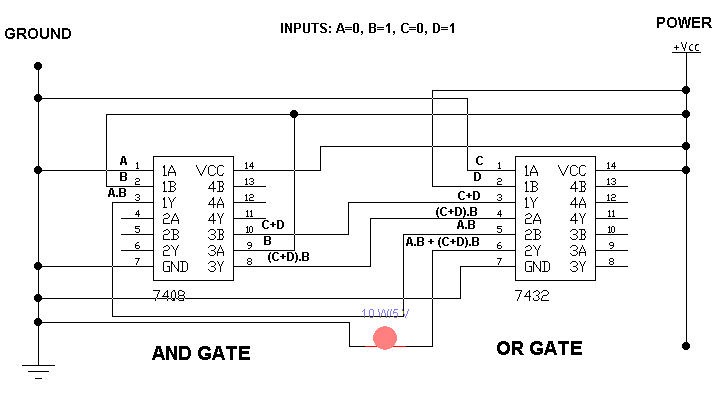
AND GATE

**Circuit Diagram:**

FOR A.B + B.C + B.D

****

FOR A.B + (C + D).B

****

**Result:**

LED Turns on only when one of combinations i.e. A.B, B.C and B.D, is 1

**PRACTICAL # 3**

**OBJECTIVE:**

To study and verifying the working of De Morgan’s Law i.e.

**ICS:**

* IC 74LS08 (AND GATE)
* IC 74LS32 (OR GATE)
* IC 74LS04 (NOT GATE)

**Apparatus:**

* Bread board
* LED
* wires
* DC supply

**Circuit Symbols:**

OR GATE

NOT GATE

AND GATE

****

**FOR :**

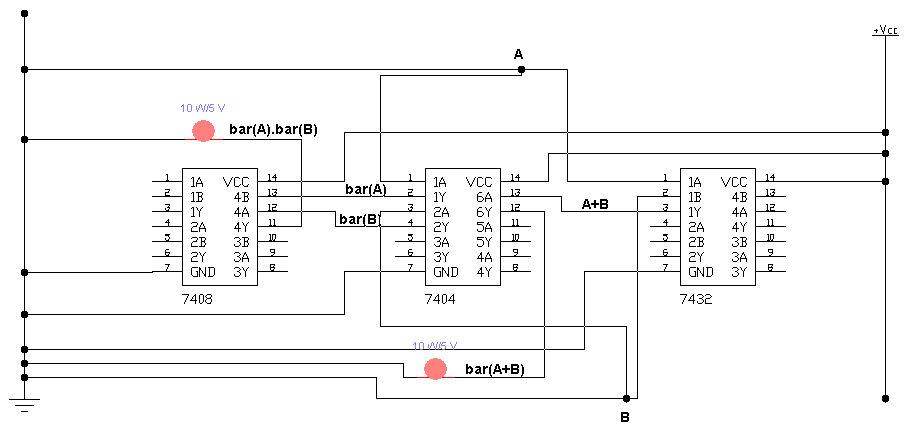
**Procedure:**

First place AND, OR and NOT ICs on the breadboard. Connect 7th pin to ground and 14th pin to voltage of each ICs. Give input A to 1st pin of OR and NOT gate both and input B to 3rd and 2nd pin of NOT and OR Gate both respectively. Connect 3rd pin of OR Gate which is A+B to 13th pin of NOT gate and connect bulb1 to 12th pin of NOT gate. Connect 2nd and 4th pin, which is and , to 13th and 12th pin of AND gate respectively and connect bulb2 to its 11th pin. Now give input to A and B according to the following truth table.

**Truth Table:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **A** | **B** |  |  | **A+B** |  |  |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 |

**Circuit Diagram:**

****

**Result:**

LED Turns on only when both inputs is 0

**FOR**

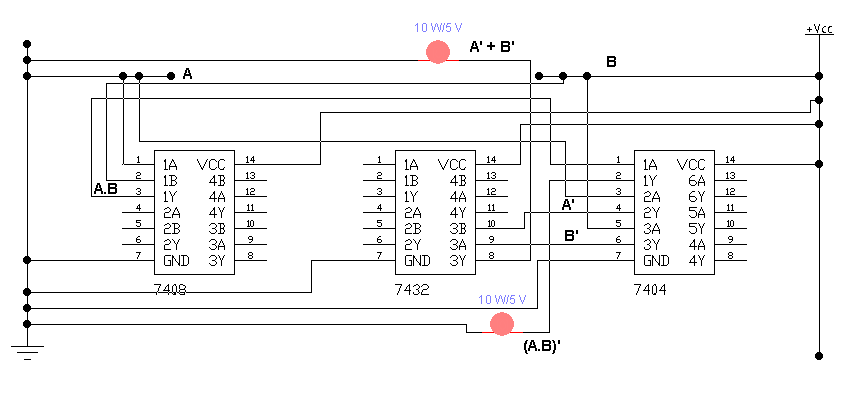
**Procedure:**

First place AND, OR and NOT ICs on the breadboard. Connect 7th pin to ground and 14th pin to voltage of each ICs. Give input A to 1st pin of AND and 3rd pin of NOT gate both and input B to 2nd and 5th pin of AND and NOT Gate both respectively. Connect 3rd pin of AND Gate which is A.B to 1st pin of NOT gate and connect bulb1 to 2nd pin of NOT gate. Connect 4th and 6th pin, which is and , to 10th and 9th pin of OR gate respectively and connect bulb2 to its 8th pin. Now give input to A and B according to the following truth table.

**Truth Table:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **A** | **B** |  |  | **A.B** |  |  |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 |

**Circuit Diagram:**

****

**Result:**

LED Turns off only when both inputs is 1

**PRACTICAL # 4**

**OBJECTIVE:**

To study the working of following equation i.e.

**ICS:**

* IC 74LS08 (AND GATE)
* IC 74LS32 (OR GATE)
* IC 74LS04 (NOT GATE)

**Apparatus:**

* Bread board
* LED
* wires
* DC supply

**Circuit Symbols:**

OR GATE

NOT GATE

AND GATE

****

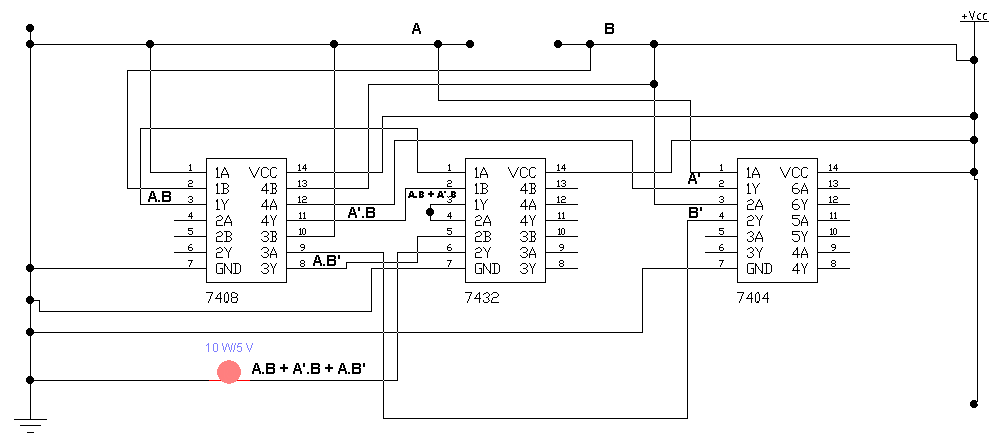
**Procedure:**

First place AND, OR and NOT ICs on the breadboard. Connect 7th pin to ground and 14th pin to voltage of each ICs. Give input A to 1st and 10th pin of AND gate and 1st pin of NOT gate. Give input B to 2nd and 13th pin of AND gate and 3rd pin of NOT gate. Connect 3rd, 11th and 8th pin of AND gate to 1st, 2nd and 5th pin of OR gate respectively. Connect 3rd pin of OR gate to its 4th pin. Connect 2nd and 4th pin of NOT gate to 12th and 9th pin of AND gate respectively. Connect bulb at 6th pin of OR gate. Now provide inputs A and B according to the following truth table

**Truth Table:**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **A** | **B** |  |  | **AB** |  |  |  |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |

**Circuit Diagram:**

****

**Result:**

LED Turns off only when both inputs is 0

**PRACTICAL # 5**

**OBJECTIVE:**

Using an IC of AND/OR gate convert two input-gate to five input-gate

**IC:**

* IC 74LS08 (AND GATE) / IC 74LS32 (OR GATE)

**Apparatus:**

* Bread board
* LED
* wires
* DC supply

**Circuit Symbols:**

OR GATE

AND GATE

****

**Procedure:**

First place AND/OR gate on the bread board. Connect 7th and 14th pin to the negative and positive terminal respectively. Give input A, B, C, D and E to the 1st, 2nd, 5th, 12th and 9th pin respectively. Connect 3rd pin to 4th pin, 6th pin to 13th pin and 11th pin to 10th pin. Connect a bulb to 8th pin. Now, give inputs A, B, C, D and E as per the following truth table

**Truth Table:**

FOR AND GATE

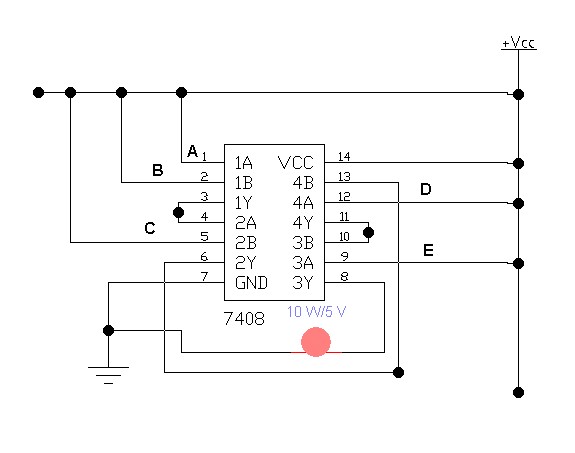
|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **E** | **A.B** | **A.B.C** | **A.B.C.D** | **A.B.C.D.E** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

FOR OR GATE

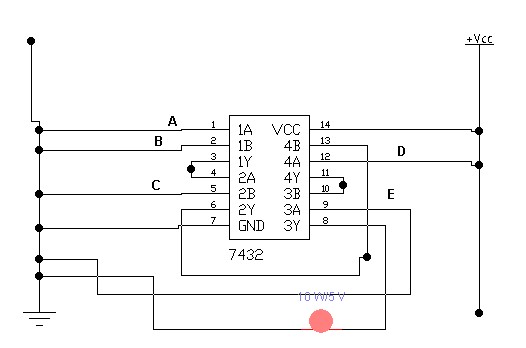
|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **E** | **A+B** | **A+B+C** | **A+B+C+D** | **A+B+C+D+E** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Circuit Diagram:**

For AND gate



For OR gate



**Result:**

For AND gate: LED turns on only when all five inputs are 1.

For OR gate: LED turns on only when one of five inputs is 1.

**PRACTICAL # 6**

**OBJECTIVE:**

To study and obtain the simplified equation from the following Karnaugh-Map:



|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  |  |  |  |
|  | 1 |  |  |  |
|  | 1 | 1 | 1 |  |
|  | 1 | 1 | 1 | 1 |
|  | 1 |  |  |  |

**ICS:**

* IC 74LS08 (AND GATE)
* IC 74LS32 (OR GATE)
* IC 74LS04 (NOT GATE)

**Apparatus:**

* Bread board
* LED
* wires
* DC supply

**Circuit Symbols:**

OR GATE

NOT GATE

AND GATE

****

**Extract Simplified Equation:**

1. Grouping of ones

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  |  |  |  |
|  | 1 |  |  |  |
|  | 1 | 1 | 1 |  |
|  | 1 | 1 | 1 | 1 |
|  | 1 |  |  |  |

1. Extract Equation:

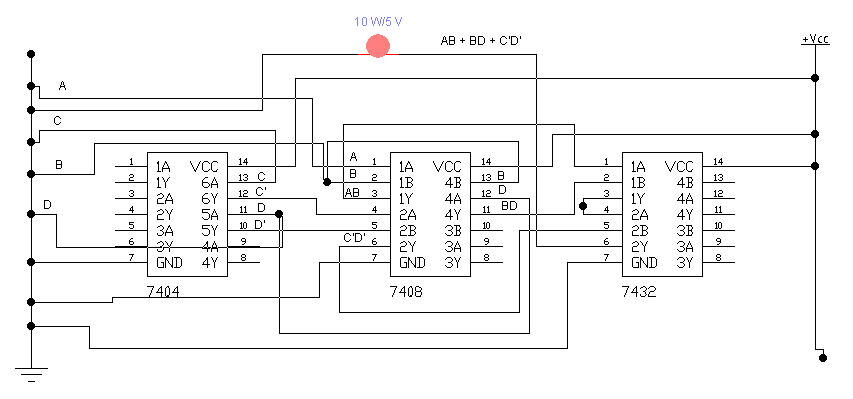
**Procedure:**

First place AND, OR and NOT ICs on the breadboard. Connect 7th pin to ground and 14th pin to voltage of each ICs. Give inputs A, B, C and D to 1st and 2nd of AND gate 13th and 11th pins of NOT Gate respectively. Connect 2nd pin of AND gate, which is B, to 13th pin of AND gate and 11th pin of NOT gate, which is D, to 12th pin of AND gate. Connect 12th and 10th pin of NOT gate, which is C and D, to 4th and 5th pin of AND gate, Connect 3rd , 11th and 6th pin of AND gate, which is AB, BD and to 1st, 2nd, and 5th pin of OR gate respectively. Now give inputs to A, B, C and as per the following truth table.

**Truth Table:**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** |  |  |  |  |  |  |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |

**Circuit Diagram:**



**Result:**

LED turns on only when all inputs is zero or when all inputs is one or when only B or A is one or when only B and D or A and B is one or when only B, C and D or A, B and D or A, B and C is one.

**PRACTICAL # 7**

**OBJECTIVE:**

To construct truth table for **2** where x is a 3-bit input and Design a Karnaugh map for the truth table and design circuit for minimized expression

**ICS:**

* IC 74LS08 (AND GATE)
* IC 74LS32 (OR GATE)
* IC 74LS04 (NOT GATE)
* IC 74LS86 (XOR GATE)

**Apparatus:**

* Bread board
* LED
* wires
* DC supply

**Circuit Symbols:**

NOT GATE

AND GATE

****

XOR GATE

OR GATE

****

**Procedure:**

We have to implement all the outputs in the breadboard. We take one XOR, NOT, OR, and 2 AND gate named AND1 and AND2. Give input A to pin 2 of XOR gate and to 1st, 4th, and 10th pin of AND1. Give input B to 13th pin of NOT gate, to 1st pin of XOR gate, to 2nd pin of AND1 gate and to 1st pin of AND2 gate. Give input C to 9th pin of NOT gate and to 12th pin of AND1 gate. Connect 12th pin of NOT gate to 5th pin of AND1 gate. Connect 8th pin of NOT gate to 9th pin of AND1 and 2nd pin of AND2 gate. Connect 6th and 8th pin of AND1 to 1st and 2nd pin of OR gate respectively.

Connect 3rd pin of XOR gate to 13th pin of AND1 gate. Get y0 and y2 from 3rd and 11th pin of AND1 respectively, y1 from 3rd pin of OR, y3 from 3rd pin from AND2 and y5 from input C. Give inputs according to the following truth table.

**Truth Table:**

First we have to find the number of output.

No. of output = No. of digit in binary of function([2^(No. of input)-1])

Here function is f(x) = x2 and No. of input is 3

No. of output = No. of digit in binary of function(7)

No. of output = No. of digit in binary of 49

No. of output = No. of digit in 110001 = 6

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **X2** | **Y** | **Y0** | **Y1** | **Y2** | **Y3** | **Y4** | **Y5** |
| 0 | 0 | 0 | 02 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 12 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 22 | 4 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 32 | 9 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 42 | 16 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 52 | 25 | 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 62 | 36 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 72 | 49 | 1 | 1 | 0 | 0 | 0 | 1 |

K-Map for Y0

|  |  |  |
| --- | --- | --- |
|  |  |  |
|  | 0 | 0 |
|  | 0 | 0 |
|  | 1 | 1 |
|  | 0 | 0 |

Y0 = AB

K-Map for Y1

|  |  |  |
| --- | --- | --- |
|  |  |  |
|  | 0 | 0 |
|  | 0 | 0 |
|  | 0 | 1 |
|  | 1 | 1 |

Y1 = +

K-Map for Y2

|  |  |  |
| --- | --- | --- |
|  |  |  |
|  | 0 | 0 |
|  | 0 | 1 |
|  | 0 | 0 |
|  | 0 | 1 |

Y2 = + = =

K-Map for Y3

|  |  |  |
| --- | --- | --- |
|  |  |  |
|  | 0 | 0 |
|  | 1 | 0 |
|  | 1 | 0 |
|  | 0 | 0 |

Y3 =

K-Map for Y4

|  |  |  |
| --- | --- | --- |
|  |  |  |
|  | 0 | 0 |
|  | 0 | 0 |
|  | 0 | 0 |
|  | 0 | 0 |

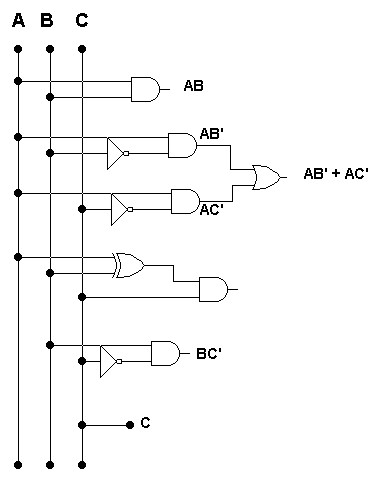
Y4 = 0

K-Map for Y5

|  |  |  |
| --- | --- | --- |
|  |  |  |
|  | 0 | 1 |
|  | 0 | 1 |
|  | 0 | 1 |
|  | 0 | 1 |

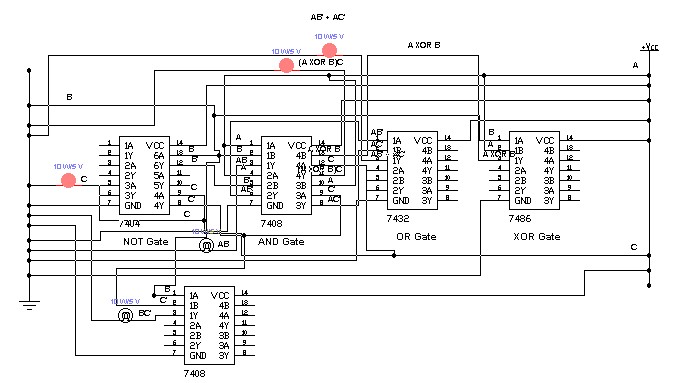
Y5 =

**Circuit Diagram:**



**B) C**

**B**



**Result:**

Maximum no of ON output at a time is 3 when all inputs is one or A and B is one.

**PRACTICAL # 8**

**OBJECTIVE:**

To study and implement the half adder and full adder

**ICS:**

* IC 74LS08 (AND GATE)
* IC 74LS32 (OR GATE)
* IC 74LS86 (XOR GATE)

**Apparatus:**

* Bread board
* LED
* wires
* DC supply

**Circuit Symbols:**

AND GATE

XOR GATE

OR GATE

****

**Procedure:**

*Definition*: Adder is used to represent binary addition which includes a carry and an actual result which is called sum here. For example, in 1+1 the actual result is zero but carry is one. There are two types of Adders. Half Adder: It is used when no. of input is maximum two and contain one bit only, and Full Adder: It is used to when no. of input is 3 and contains one bit only each.

*Half Adder:* We take a XOR and an AND gate. Give input A and B to 1st pin of both gates and 2nd pin of both gates respectively. Take Sum from 3rd pin XOR gate and carry from 3rd pin of AND gate.

**B**

Sum =

Carry = AB

*Full Adder:* We take a XOR, OR and an AND gate. Give input A to 1st and 13th pin of XOR and AND gate respectively. Give input B to 2nd and 12th pin of XOR and AND gate respectively. Give input C to 4th and 2nd pin of XOR and AND gate respectively. Connect 3rd pin of XOR gate to 5th pin of itself and to 1st pin of AND gate. Connect 3rd and 11th pin of AND gate to 1st and 2nd pin of OR gate respectively. Take Sum from 6th pin of XOR gate and Carry from 3rd pin of OR gate.

Sum =

Carry =

**Truth Table:**

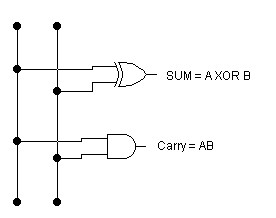
Half Adder

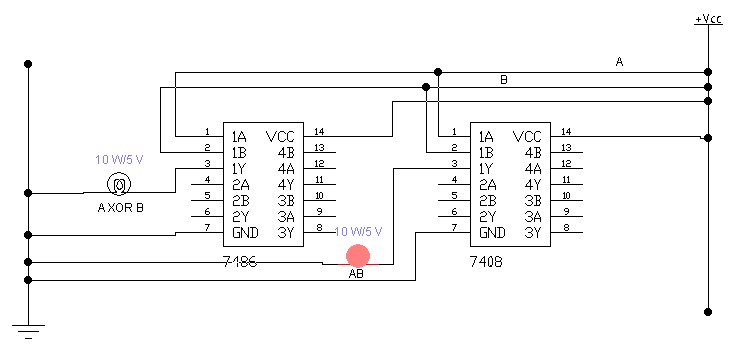
|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **B** | **Carry** | **Sum** |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Full Adder

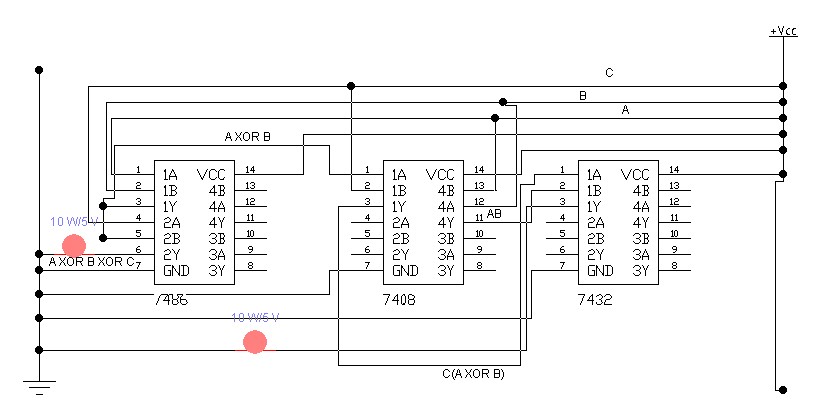
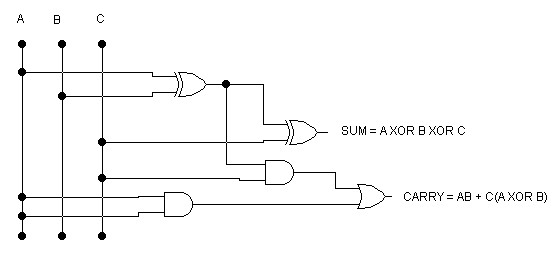
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **Carry** | **Sum** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |

**Circuit Diagram:**

Half Adder



Full Adder



**Result:**

We use Half Adder when we have two no. of input which contain only one bit and we use Full Adder when we have three no. of input which contain only one bit.

**PRACTICAL # 9**

**OBJECTIVE:**

To study and implement the parallel adder i.e. combination of half adder and full adder

**ICS:**

* IC 74LS08 (AND GATE)
* IC 74LS32 (OR GATE)
* IC 74LS86 (XOR GATE)

**Apparatus:**

* Bread board
* LED
* wires
* DC supply

**Circuit Symbols:**

AND GATE

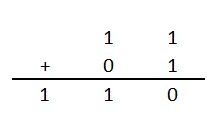
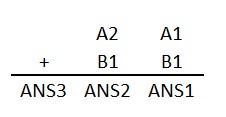
XOR GATE

OR GATE

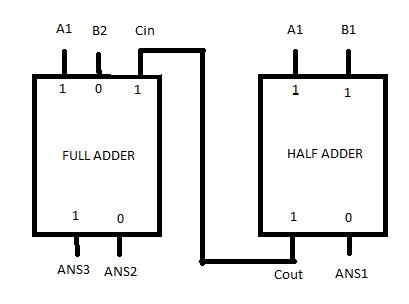
****

**Procedure:**

We have to add two number. E.g.

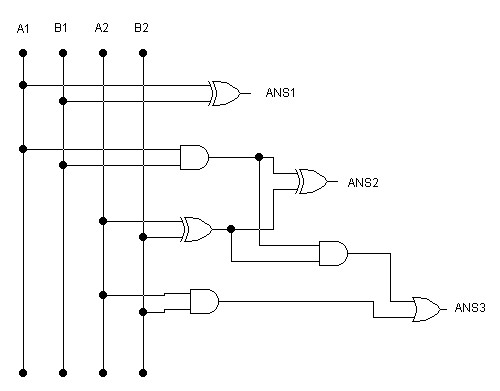


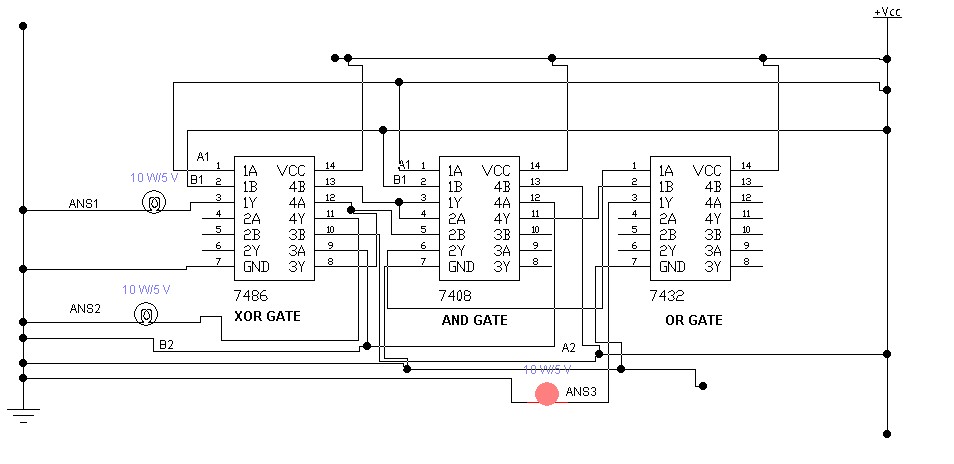
First, we use half adder and then full adder.



Firstly we connect A1 and B1 to 1st and 2nd pin of XOR and AND gate both respectively. Then connect A2 to 10th pin of XOR gate and 13th pin of AND gate and B2 to 9th pin of XOR gate and 12th pin of AND gate. Then connect 3rd pin of AND gate to 4th pin of AND gate and 13th pin of XOR gate. Then connect 8th pin of XOR gate to 12th pin of XOR gate and 5th pin of AND gate. Then connect 6th and 11th pin of AND gate to 1st and 2nd pin of OR gate respectively. Then get answer ANS1, ANS2 and ANS3 at 3rd pin of XOR gate, 11th pin of XOR gate and 3rd pin of OR gate respectively.

**Circuit Diagram:**

****

****

**Result:**

We get 1 on ANS3 and 0 on ANS1 and ANS2 both.